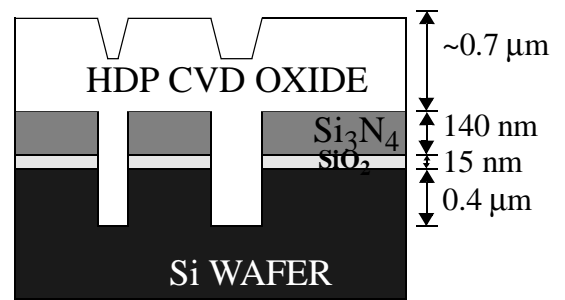
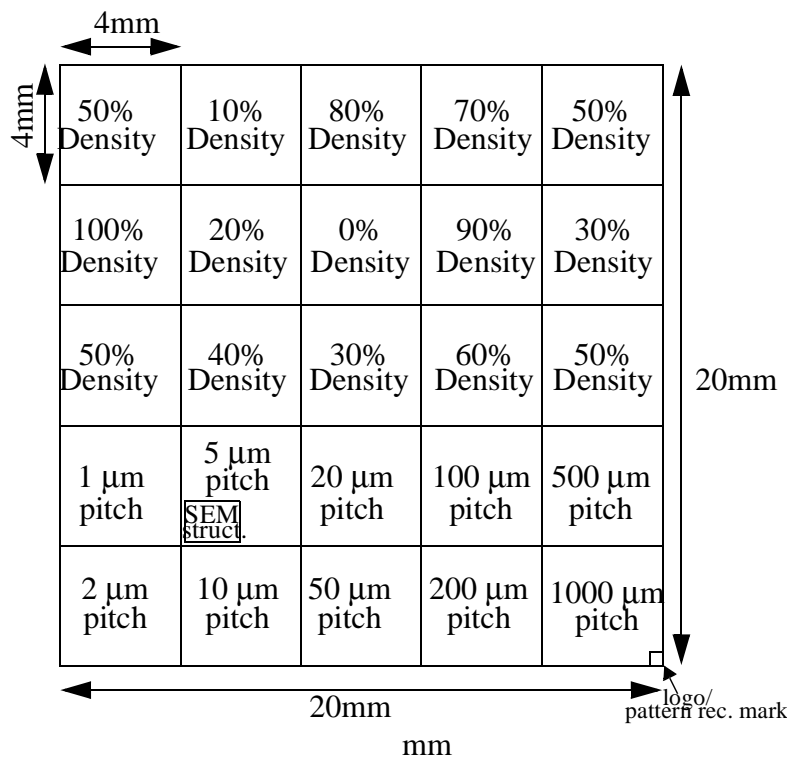


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SKW 3-2 Wafer Specifications

DATE: March 14, 2002



Cross Sectional View

SKW3-2 Mask Floor Plan

PARAMETER	NOMINAL	TOLERANCE
Patterning		
Center Die X Location	-10.000 mm	+/- 100 μm
Center Die Y Location	-10.000 mm	+/- 100 μm
Die Size: X	20 mm	+/- 10 μm
Die Size: Y	20 mm	+/- 10 μm
Die Spacing	120 μm/120 μm	+/- 10 μm

Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on wafer unpatterned. (Under certain stepper operating conditions, 2mm edge exclusion is allowed.)		
<i>Linewidth Variation</i> (measured on 10 μm and 90 μm structures)		
Lot-to-Lot	10 μm , 90 μm	+/- 1 μm
Within-Lot (Wafer-to-Wafer)		+/- 1 μm
Within-Wafer		+/- 1 μm
Within-Die		+/- 1 μm
<i>Raisde Area Thickness (HDP CVD Oxide Fill)</i>		
Lot-to-Lot	0.7 μm	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
<i>Raised Area Thickness (Nitride)</i>		
Lot-to-Lot	1400 \AA	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
<i>Raised Area Thickness (Pad Oxide)</i>		
Lot-to-Lot	150 \AA	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
<i>Silicon Trench Depth</i>		
Lot-to-Lot	4000 \AA	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 10 %
Within-Die		+/- 10 %