

SKW Associates, Inc.

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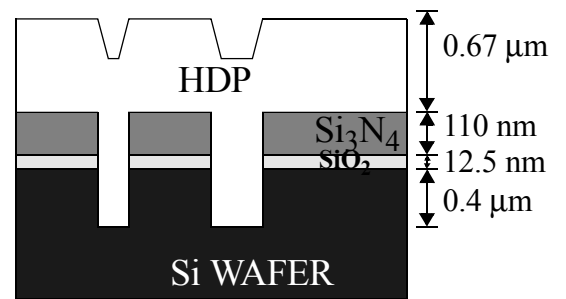
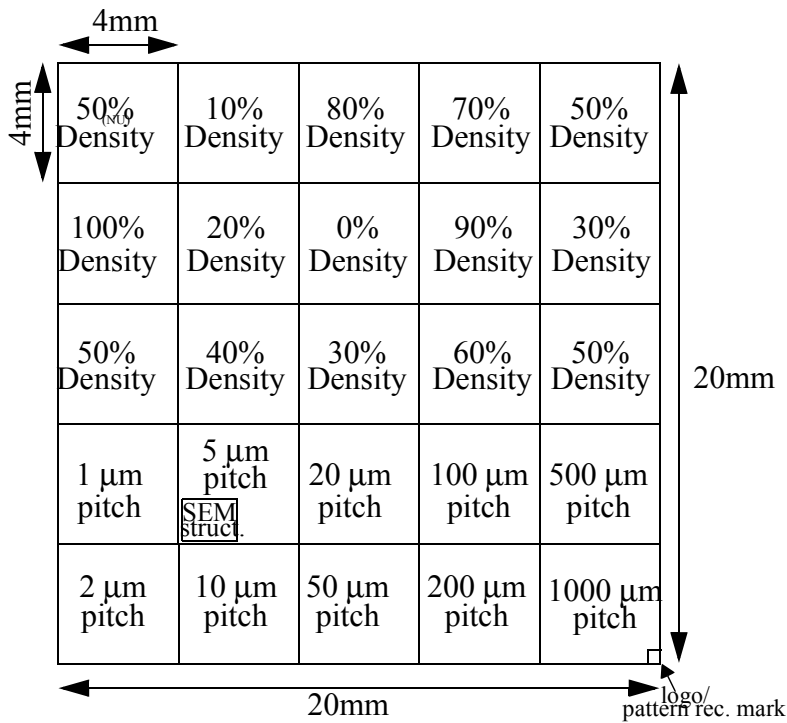
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SKW 3-2C-6700 HDP 300mm Wafer Specifications

DATE: Oct 7, 2004



Cross Sectional View

SKW3-2 Mask Floor Plan

Pad Oxide Deposition

PARAMETER	NOMINAL	TOLERANCE
Pad Oxide (SiO₂) Thickness		
Lot-to-Lot	125 Å	+/- 5%
Within-Lot (Wafer-to-Wafer)		+/- 5%
Within -Wafer		+/- 5%
Within-Die		+/- 5%

Nitride Deposition

PARAMETER	NOMINAL	TOLERANCE
<i>Nitride (Si₃N₄) Thickness</i>		
Lot-to-Lot	1100 Å	+/- 5%
Within-Lot (Wafer-to-Wafer)		+/- 5%
Within-Wafer		+/- 5%
Within-Die		+/- 5%

Patterning

PARAMETER	NOMINAL	TOLERANCE
<i>Patterning</i>		
Center Die X Location	-10.000 mm	+/- 100 µm
Center Die Y Location	-10.000 mm	+/- 100 µm
Die Size: X	20 mm	+/- 10 µm
Die Size: Y	20 mm	+/- 10 µm
Die Spacing	115 µm	+/- 10 %
Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on wafer unpatterned. (Under certain stepper operating conditions, 2mm or more edge exclusion is allowed.)		
<i>Linewidth Variation</i> (measured on 2 µm structures)		
Lot-to-Lot	2 µm	+/- 0.1 µm
Within-Lot (Wafer-to-Wafer)		+/- 0.1 µm
Within-Wafer		+/- 0.1 µm
Within-Die		+/- 0.1 µm

Etch

PARAMETER	NOMINAL	TOLERANCE
<i>Step-Height / Trench Depth</i> (2 µm, 100 µm, 10%, & 90% structures)		
Lot-to-Lot	0.4 µm	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %

Within-Wafer		+/- 5 %
Within-Die		+/- 5 %

HDP CVD Oxide Deposition

PARAMETER	NOMINAL	TOLERANCE
<i>Oxide Thickness</i> (2 μm, 100 μm, 10%, & 90% structures)		
Lot-to-Lot	0.67 μm	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %