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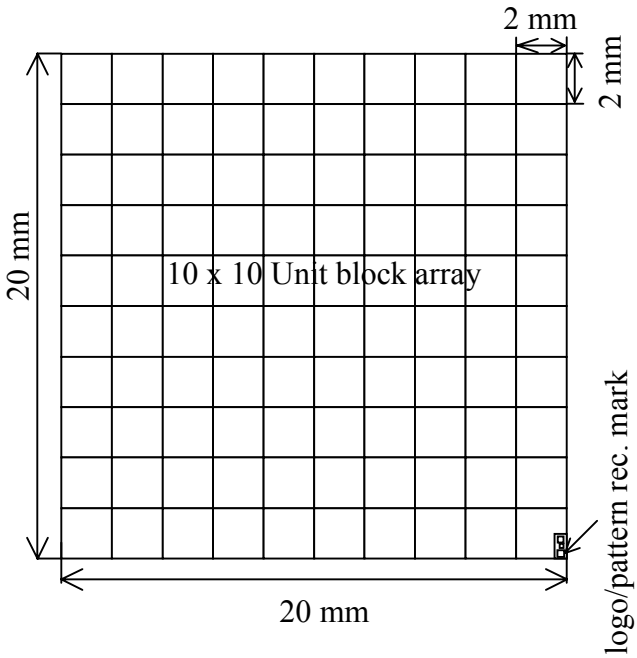
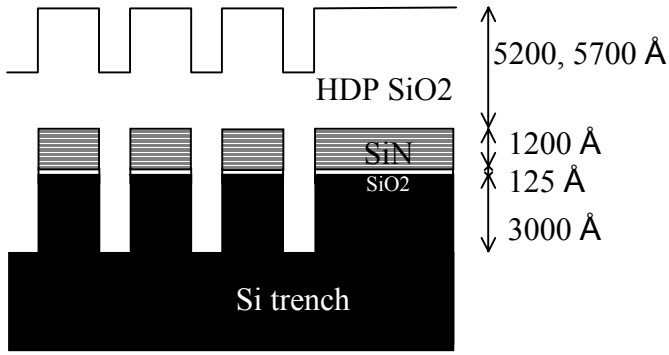
SKW 3-5 Wafer Specifications

DATE: May 15, 2004



SKW 3-5 Mask Floor Plan



Cross Sectional View

PARAMETER	NOMINAL	TOLERANCE
Patterning		
Center Die X Location	-10.000 mm	+/- 10 µm
Center Die Y Location	-10.000 mm	+/- 10 µm
Die Size: X	20 mm	+/- 10 µm
Die Size: Y	20 mm	+/- 10 µm
Die Stepping	20 µm	+/- 100 µm
Wafers must be patterrned all the way to the edges of the wafer, i.e. no area anywhere on the wafer unpatterned. (Under certain stepper operating conditions, 2 mm edge edge exclusion is allowed.)		

PARAMETER	NOMINAL	TOLERANCE
CD Variation (measured on shallow strenches)		
Lot-to-Lot	250 nm	+/- 10 nm
Within-Lot (Wafer-to-Wafer)		+/- 10 nm
Within-Wafer		+/- 10 nm
Within-Die (measured on 9 trneches)		+/- 14 nm
Raised area thcikness (HDP CVD Oxide fill)		
Lot-to-Lot	5200 or 5700 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
Raised area thcikness (Nitride)		
Lot-to-Lot	1200 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
Raised area thcikness (Pad Oxide)		
Lot-to-Lot	125 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
Silicon Trench Depth		
Lot-to-Lot	3000 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 10 %
Within-Die		+/- 10 %