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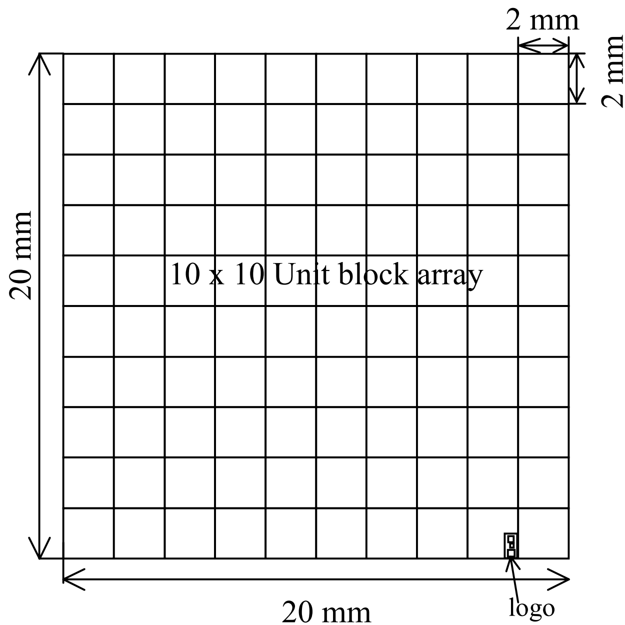
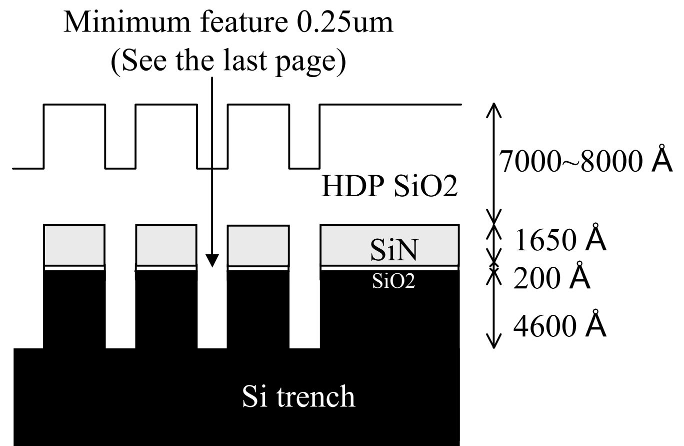
SKW 3-6 *300mm* Wafer Specifications

DATE: Feb 16, 2004



SKW 3-6 Mask Floor Plan



Cross Sectional View

PARAMETER	NOMINAL	TOLERANCE
Patterning		
Center Die X Location	-10.000 mm	+/- 10 µm
Center Die Y Location	-10.000 mm	+/- 10 µm
Die Size: X	20 mm	+/- 10 µm
Die Size: Y	20 mm	+/- 10 µm
Die Stepping (X /Y)	460 / 20 µm	+/- 100 µm
Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on the wafer unpatterned. (Under certain stepper operating conditions, 2 mm edge edge exclusion is allowed.)		

PARAMETER	NOMINAL	TOLERANCE
CD Variation (measured on shallow trenches)		
Lot-to-Lot	250 nm	+/- 10 nm
Within-Lot (Wafer-to-Wafer)		+/- 10 nm
Within-Wafer		+/- 10 nm
Within-Die (measured on 9 trenches)		+/- 14 nm
Raised area thickness (HDP CVD Oxide fill)		
Lot-to-Lot	8000 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
Raised area thickness (Nitride)		
Lot-to-Lot	1650 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
Raised area thickness (Pad Oxide)		
Lot-to-Lot	200 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
Silicon Trench Depth		
Lot-to-Lot	4600 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 10 %
Within-Die		+/- 10 %
Pre-CMP defect		
Within-Wafer (2 wafers per Lot)	<160nm	<200 ea

- Pre-CMP defect data are provided together with measurement conditions.
- We believe LSI Logic’s metrology engineers will have better ideas for actual measurements. We will follow their suggestions and provide their metrology recipes to our customers. We hope your company has KLA-Tencor AIT-II system or equivalent.