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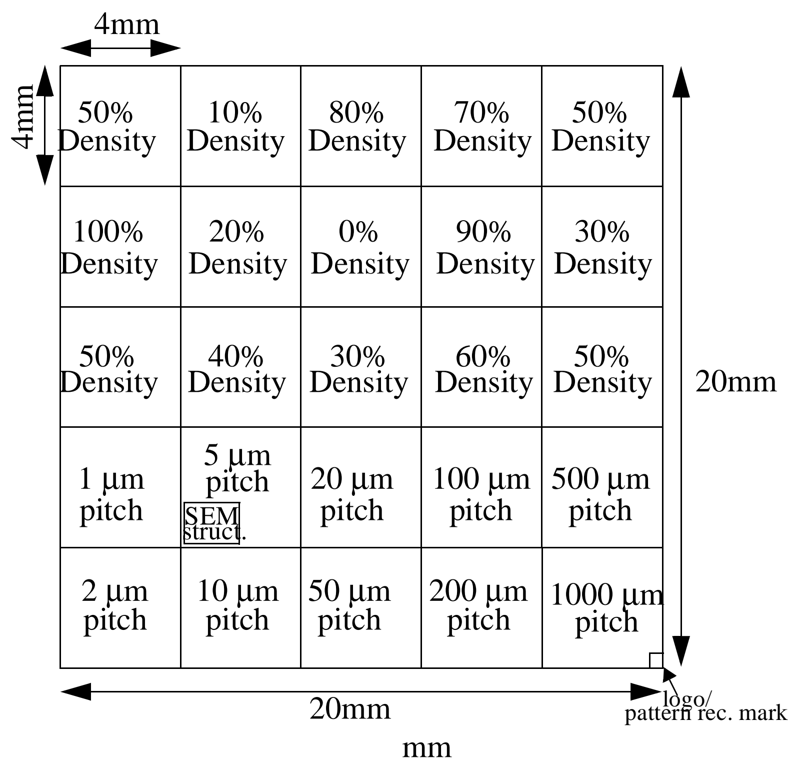
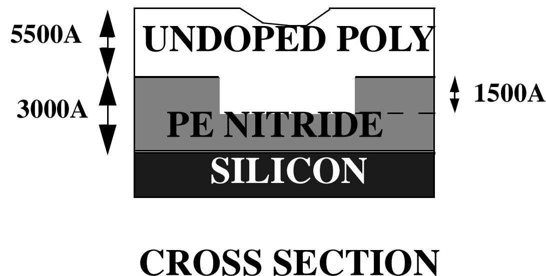
SKW 3PN Wafer Specifications

DATE: April 17, 2003



SKW3PN Mask Floor Plan



CROSS SECTION

PARAMETER	NOMINAL	TOLERANCE
Patterning		
Center Die X Location	-10.000 mm	+/- 100 µm
Center Die Y Location	-10.000 mm	+/- 100 µm
Die Size: X	20 mm	+/- 10 µm
Die Size: Y	20 mm	+/- 10 µm
Die Spacing	120 µm/120 µm	+/- 100 µm

Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on wafer unpatterned. (Under certain stepper operating conditions, 2mm edge exclusion is allowed.)		
Linewidth Variation (measured on 10 µm and 90 µm structures)		
Lot-to-Lot	10 µm, 90 µm	+/- 1 µm
Within-Lot (Wafer-to-Wafer)		+/- 1 µm
Within-Wafer		+/- 1 µm
Within-Die		+/- 1 µm
Raised Area Thickness (Undoped PolySilicon Fill)		
Lot-to-Lot	0.55 µm	+/- 8 %
Within-Lot (Wafer-to-Wafer)		+/- 8 %
Within-Wafer		+/- 8 %
Within-Die		+/- 8 %
Raised Area Thickness (PE Nitride)		
Lot-to-Lot	0.3 µm	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
Oxide Trench Depth		
Lot-to-Lot	1500 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5%
Within-Die		+/- 5 %