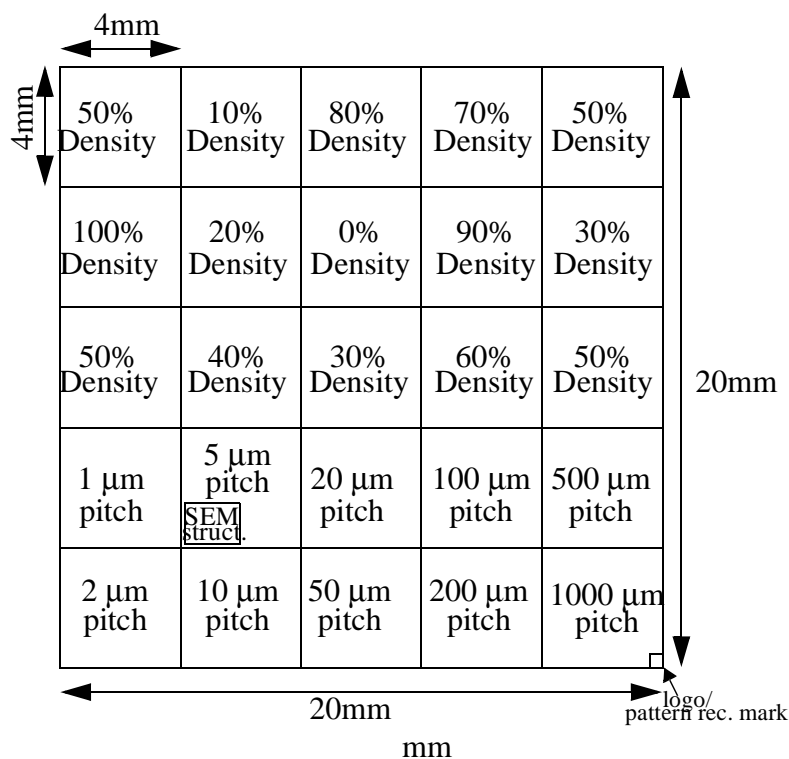


# SKW Associates, Inc.

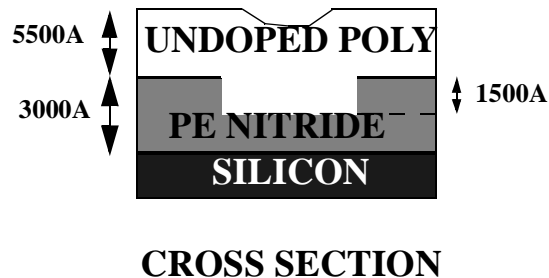
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# SKW 3PN Wafer Specifications

DATE: April 17, 2003



**SKW3PN Mask Floor Plan**



PARAMETER	NOMINAL	TOLERANCE
<b>Patterning</b>		
Center Die X Location	-10.000 mm	+/- 100 $\mu\text{m}$
Center Die Y Location	-10.000 mm	+/- 100 $\mu\text{m}$
Die Size: X	20 mm	+/- 10 $\mu\text{m}$
Die Size: Y	20 mm	+/- 10 $\mu\text{m}$
Die Spacing	120 $\mu\text{m}$ /120 $\mu\text{m}$	+/- 100 $\mu\text{m}$

<b>Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on wafer unpatterned. (Under certain stepper operating conditions, 2mm edge exclusion is allowed.)</b>		
<b><i>Linewidth Variation</i></b> (measured on 10 $\mu\text{m}$ and 90 $\mu\text{m}$ structures)		
Lot-to-Lot	10 $\mu\text{m}$ , 90 $\mu\text{m}$	+/- 1 $\mu\text{m}$
Within-Lot (Wafer-to-Wafer)		+/- 1 $\mu\text{m}$
Within-Wafer		+/- 1 $\mu\text{m}$
Within-Die		+/- 1 $\mu\text{m}$
<b><i>Raised Area Thickness (Undoped PolySilicon Fill)</i></b>		
Lot-to-Lot	0.55 $\mu\text{m}$	+/- 8 %
Within-Lot (Wafer-to-Wafer)		+/- 8 %
Within-Wafer		+/- 8 %
Within-Die		+/- 8 %
<b><i>Raised Area Thickness ( PE Nitride )</i></b>		
Lot-to-Lot	0.3 $\mu\text{m}$	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
<b><i>Oxide Trench Depth</i></b>		
Lot-to-Lot	1500 $\text{\AA}$	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5%
Within-Die		+/- 5 %