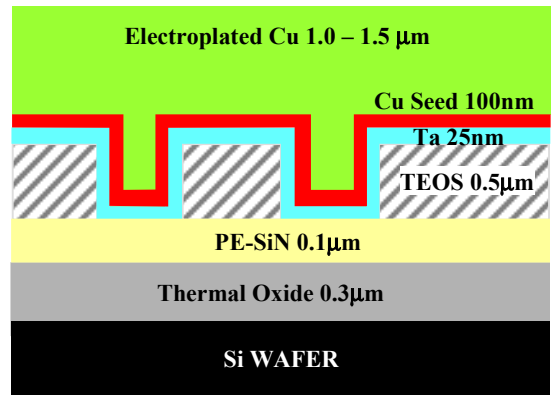
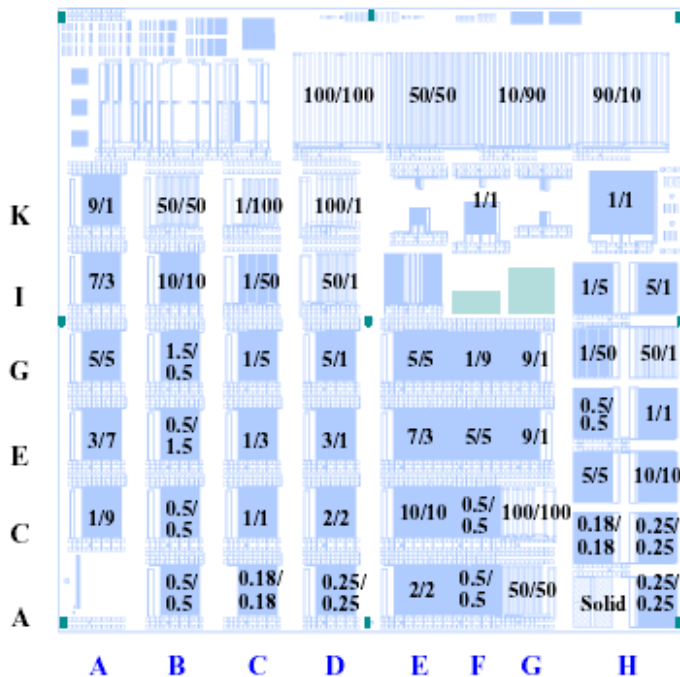


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SKW 6-3(Cu/TEOS) 300mm Wafer Specifications

DATE: November 18, 2004



Cross Sectional View

SKW6-3 (Cu/TEOS) Mask Floor Plan

Isolation Layer Deposition

1. Thermal Oxide Film Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	3000 Å	+/- 5%
Within-Lot (Wafer-to-Wafer)		+/- 5%
Within-Wafer		+/- 3%
Within-Die		+/- 3%

2. PE-SiN Film Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	1000 Å	+/- 10%
Within-Lot (Wafer-to-Wafer)		+/- 10%
Within-Wafer		+/- 5%
Within-Die		+/- 5%

3. TEOS Oxide Film Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	5000 Å	+/- 5%
Within-Lot (Wafer-to-Wafer)		+/- 5%
Within-Wafer		+/- 3%
Within-Die		+/- 3%

Metal Conducting Layer Deposition

1. Ta Film Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	250 Å	+/- 10%
Within-Lot (Wafer-to-Wafer)		+/- 10%
Within-Wafer		+/- 5%
Within-Die		+/- 5%

2. Cu Seed Layer Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	1000 Å	+/- 10%
Within-Lot (Wafer-to-Wafer)		+/- 10%
Within-Wafer		+/- 5%
Within-Die		+/- 5%

3. ECD Cu Film Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	1 µm	+/- 10%
Within-Lot (Wafer-to-Wafer)		+/- 10%
Within-Wafer		+/- 5%
Within-Die		+/- 5%

Specification for Patterning

PARAMETER	NOMINAL	TOLERANCE
Center Die X Location	-10.000 mm	+/- 100 µm
Center Die Y Location	-10.000 mm	+/- 100 µm
Die Size: X	20 mm	+/- 10 µm
Die Size: Y	20 mm	+/- 10 µm
Vertical Die Spacing	180 µm	+/- 10%
Horizontal Die Spacing	360 µm	+/- 10%

Line Width Variation (measured on 2 µm structures)

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	2 µm	+/- 0.1 µm
Within-Lot (Wafer-to-Wafer)		+/- 0.1 µm
Within-Wafer		+/- 0.1 µm
Within-Die		+/- 0.1 µm