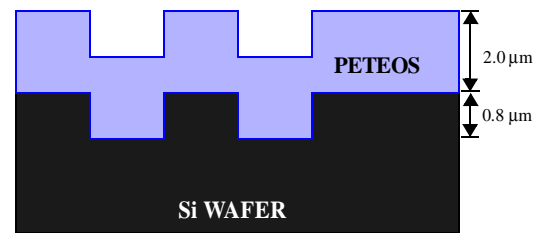
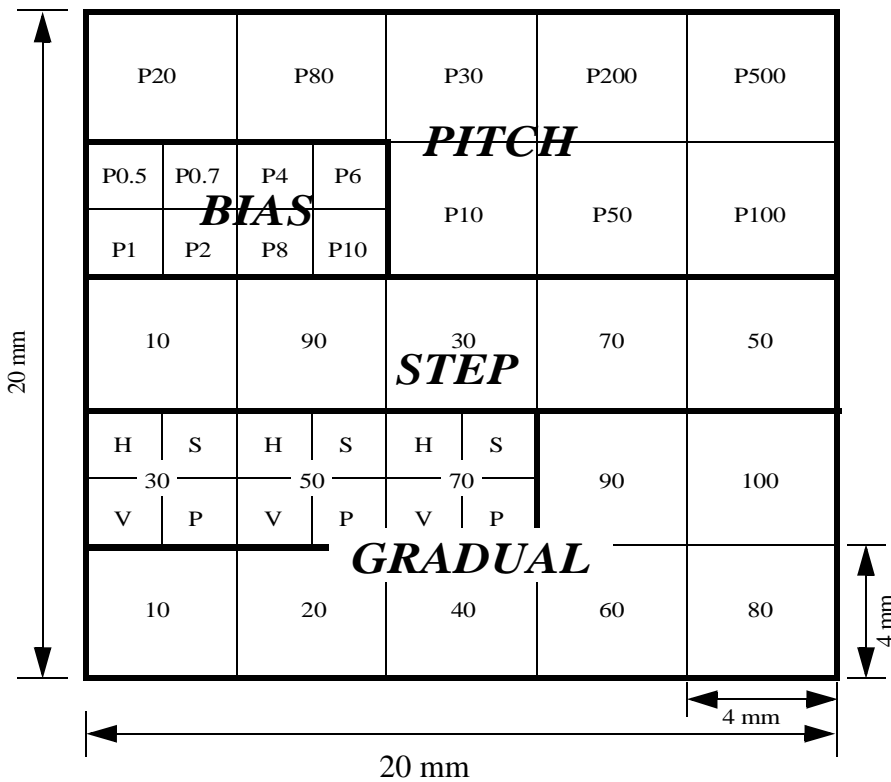


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SKW 7-2 Wafer Specifications

DATE: November 30, 2001



Wafer Cross Sectional View

SKW 7-2 Mask Floor Plan

PARAMETER	NOMINAL	TOLERANCE
Patterning		
Center Die X Location	-10.000 mm	+/- 100 μm
Center Die Y Location	-10.000 mm	+/- 100 μm
Die Size: X	20 mm	+/- 10 μm

Die Size: Y	20 mm	+/- 10 μm
Die Spacing	120 μm	+/- 10 μm
Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on wafer unpatterned. (Under certain stepper operating conditions, 2mm or more edge exclusion is allowed.)		
<i>Linewidth Variation</i> (measured on 10 μm and 90 μm structures)		
Lot-to-Lot	10 μm , 90 μm	+/- 1 μm
Within-Lot (Wafer-to-Wafer)		+/- 1 μm
Within-Wafer		+/- 1 μm
Within-Die		+/- 1 μm
<i>Thickness</i>		
Lot-to-Lot	2.0 μm	+/- 5%
Within-Lot (Wafer-to-Wafer)		+/- 5%
Within-Wafer		+/- 2%
Within-Die		+/- 2%
<i>Step-Height (Trench Depth)</i>		
Lot-to-Lot	8000 \AA	+/- 10%
Within-Lot (Wafer-to-Wafer)		+/- 10%
Within-Wafer		+/- 5%
Within-Die		+/- 5%