

GST CMP BLANKET and TEST PATTERNED WAFERS

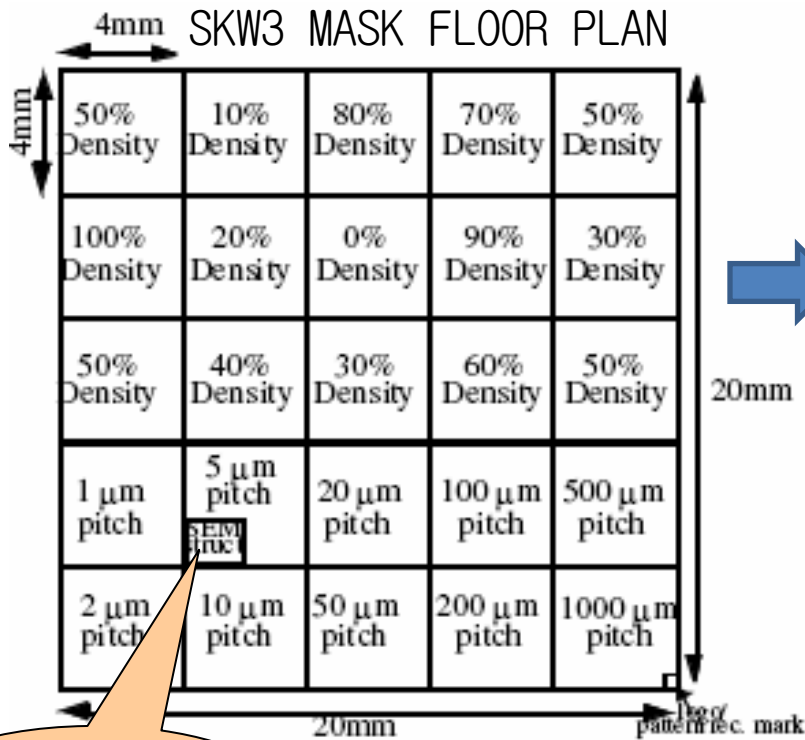
MARCH 20, 2009

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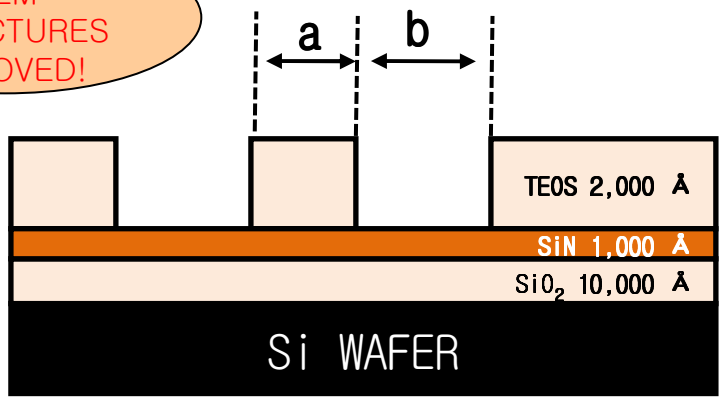
I. BLANKET FILM WAFER

- ✓ **Both 200 & 300mm Wafers Are Available**
- ✓ **Method of GST Film Deposition: PVD (Magnetron Sputtering)**
- ✓ **Typical Film Stack: Si/1kÅ SiO₂/200-300Å TiN/2.5-3kÅ GST**
- ✓ **CVD Deposition Method is Available Upon Request**
- ✓ **Deposited Surface Roughness**
 - **ATM measurement after GST 2500Å Sputtering**
 - **Scan Area: 500 μm x 500 μm**
 - **RMS 9.54Å**
 - **Ra 7.37Å**

CHANGE IN MASK LAYOUT FROM SKW3 (REMOVAL OF SEM STRUCTURES)



SEM STRUCTURES REMOVED!

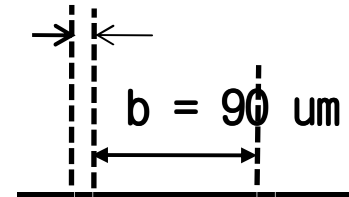


CROSS SECTIONAL VIEW

PATTERN SIZE (LINE)

a/b = 50/50 μ m	10/90	80/20	70/30	50/50
No Pattern	20/80	No pattern	90/10	30/70
50/50	40/60	30/70	60/40	50/50
0.5/0.5	2.5/2.5	10/10	50/50	250/250
1.0/1.0	5/5	25/25	100/100	500/500

a = 10 μ m



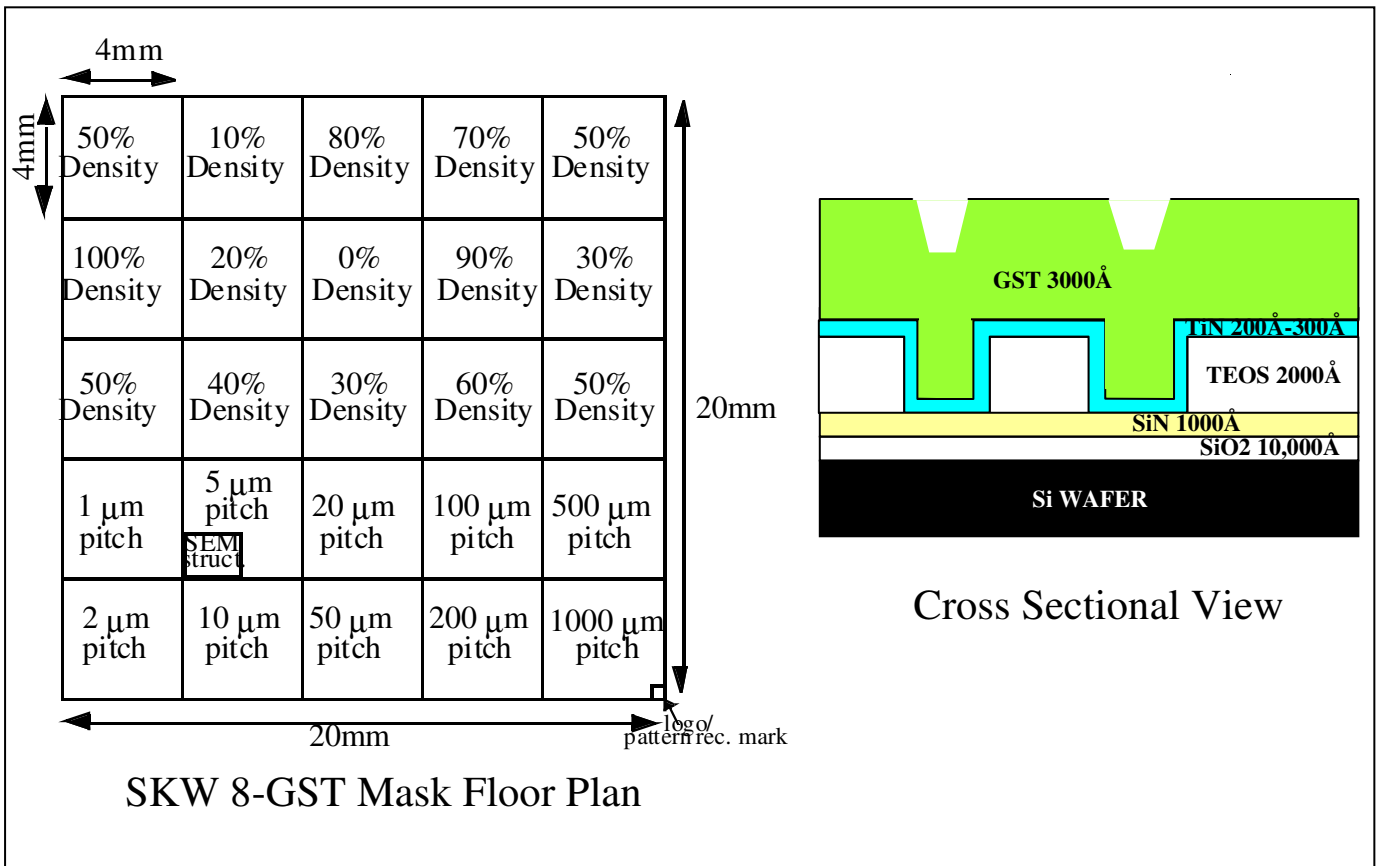
MONITORING PATTERN

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SKW 80-GST (200mm) Wafer Specifications

DATE: December 17, 2008



Specification for Patterning

PARAMETER	NOMINAL	TOLERANCE
Center Die X Location	-10.000 mm	+/- 100 μm
Center Die Y Location	-10.000 mm	+/- 100 μm
Die Size: X	20 mm	+/- 10 μm
Die Size: Y	20 mm	+/- 10 μm
Die Spacing X/Y	120 / 120 μm	+/- 10 μm
Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on wafer unpatterned. (Under certain stepper operating conditions, 2mm edge exclusion is allowed.)		

Line Width Variation (measured on 10 μm , 90 μm structures)

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	10 μm , 90 μm	+/- 0.1 μm
Within-Lot (Wafer-to-Wafer)		+/- 0.1 μm
Within-Wafer		+/- 0.1 μm
Within-Die		+/- 0.1 μm

Pad Oxide Film Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	10,000 \AA	+/- 5%
Within-Lot (Wafer-to-Wafer)		+/- 5%
Within-Wafer		+/- 3%
Within-Die		+/- 3%

SiN Film Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	1000 \AA	+/- 10%
Within-Lot (Wafer-to-Wafer)		+/- 10%
Within-Wafer		+/- 5%
Within-Die		+/- 5%

PETEOS Oxide Film Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	2000 Å	+/- 10%
Within-Lot (Wafer-to-Wafer)		+/- 10%
Within-Wafer		+/- 5%
Within-Die		+/- 5%

PVD TiN Film Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	200 Å	+/- 10%
Within-Lot (Wafer-to-Wafer)		+/- 10%
Within-Wafer		+/- 5%
Within-Die		+/- 5%

GST Film Thickness

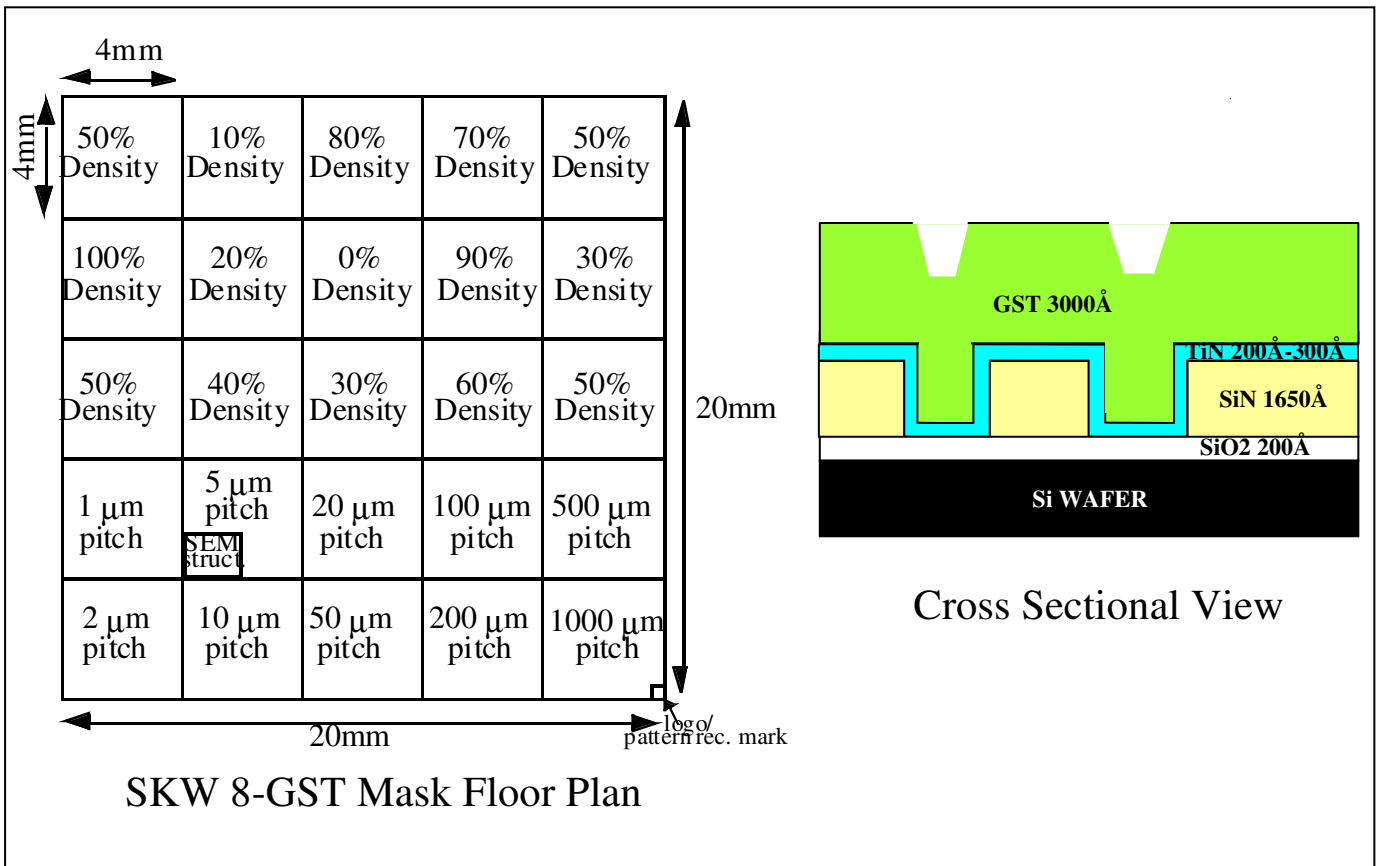
PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	3000 Å	+/- 5%
Within-Lot (Wafer-to-Wafer)		+/- 5%
Within-Wafer		+/- 3%
Within-Die		+/- 3%

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SKW 8N-GST (200mm) Wafer Specifications

DATE: December 17, 2008



Specification for Patterning

PARAMETER	NOMINAL	TOLERANCE
Center Die X Location	-10.000 mm	+/- 100 μm
Center Die Y Location	-10.000 mm	+/- 100 μm
Die Size: X	20 mm	+/- 10 μm
Die Size: Y	20 mm	+/- 10 μm
Die Spacing X/Y	120 / 120 μm	+/- 10 μm
Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on wafer unpatterned. (Under certain stepper operating conditions, 2mm edge exclusion is allowed.)		

Line Width Variation (measured on 10 μm , 90 μm structures)

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	10 μm , 90 μm	+/- 0.1 μm
Within-Lot (Wafer-to-Wafer)		+/- 0.1 μm
Within-Wafer		+/- 0.1 μm
Within-Die		+/- 0.1 μm

Pad Oxide Film Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	200 \AA	+/- 5%
Within-Lot (Wafer-to-Wafer)		+/- 5%
Within-Wafer		+/- 3%
Within-Die		+/- 3%

SiN Film Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	1650 \AA	+/- 10%
Within-Lot (Wafer-to-Wafer)		+/- 10%
Within-Wafer		+/- 5%
Within-Die		+/- 5%

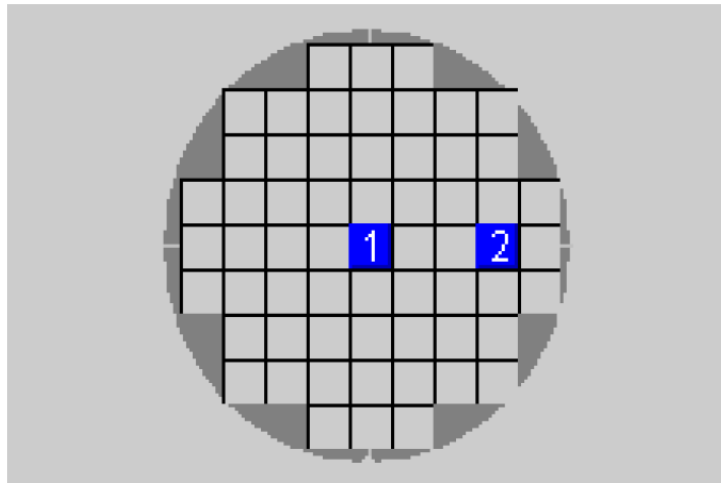
PVD TiN Film Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	200 Å	+/- 10%
Within-Lot (Wafer-to-Wafer)		+/- 10%
Within-Wafer		+/- 5%
Within-Die		+/- 5%

GST Film Thickness

PARAMETER	NOMINAL	TOLERANCE
Lot-to-Lot	3000 Å	+/- 5%
Within-Lot (Wafer-to-Wafer)		+/- 5%
Within-Wafer		+/- 3%
Within-Die		+/- 3%

SKW8-GST Dishing Characterization Location Maps



DIE LOCATIONS

50/50	10/90	80/20	70/30	50/50
No Patter n	20/80	No patter n	90/10	30/70
50/50	40/60	30/70	60/40	50/50
0.5/ 0.5 (1)	2.5/ 2.5	10/10 (4)	50/50 (5)	250/ 250
1.0/ 1.0 (2)	5/5 (3)	25/25	100/ 100 (6)	500/ 500

SITE LOCATIONS