Micro-Chevron Test Patterned Wafers For Wafer Bond Strength Characterization

SKW ASSOCIATES, INC.

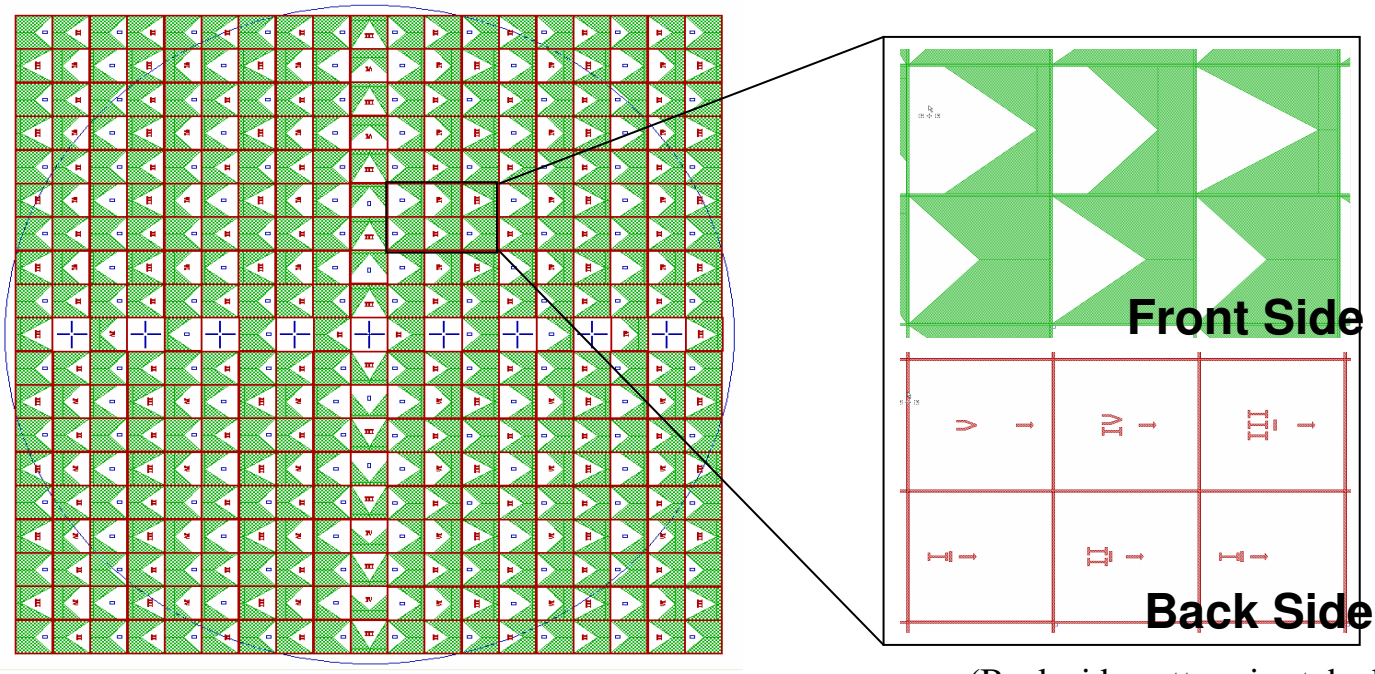
2920 Scott Blvd., Santa Clara, CA 95054

Tel: 408-919-0094, Fax: 408-919-0097

SKW Associates, Inc,
2920 Scott Blvd.
Santa Clara, CA 95054
Phone (408) 919-0094
Fax (408) 919-0097
Email: skw@testwafer.com
http//www.testwafer.com

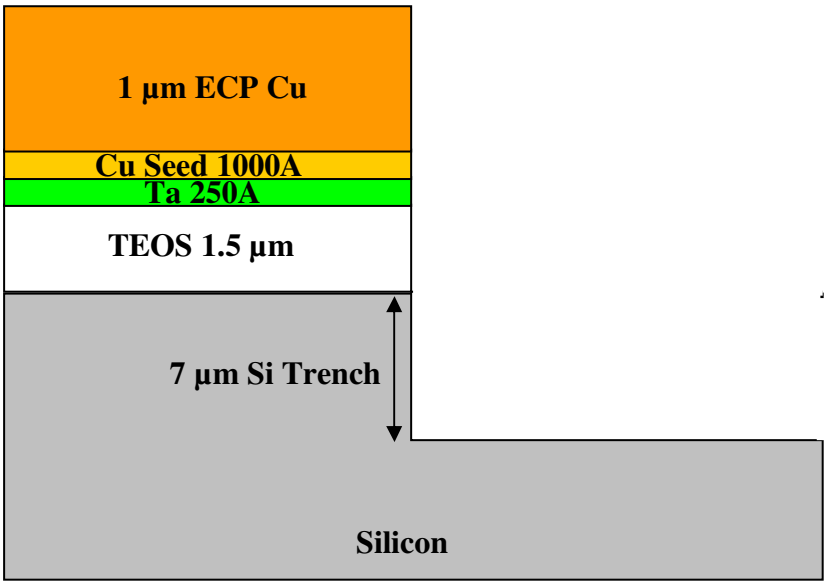
SKWBS-200-Cu-ECP Wafer Specifications

DATE: March 25, 2011



SKWBS-200-Cu-ECP Mask Layout

(Back side pattern is etched 1-2 µm into silicon for dicing reference purposes)



Cross Sectional View

PARAMETER	NOMINAL	TOLERANCE
Patterning		
Die Size: X	10 mm	+/- 10 µm
Die Size: Y	10 mm	+/- 10 µm
Die Stepping (X /Y)	200 / 200 µm	+/- 10%
Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on the wafer unpatterned. (Under certain stepper operating conditions, 2 mm edge edge exclusion is allowed.)		
TEOS Oxide film thickness		
Lot-to-Lot	1.5 µm	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 3 %
Within-Die		+/- 3 %
PVD Ta film thickness		
Lot-to-Lot	250 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
PVD Cu film thickness		
Lot-to-Lot	1000 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
ECD Cu film thickness		
Lot-to-Lot	1 µm	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %

PARAMETER	NOMINAL	TOLERANCE
Silicon trench depth		
Lot-to-Lot	7 µm	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 10 %
Within-Die		+/- 10 %
Si substrate: p-type (100), resistivity 1-100 ohm-cm, double-side polished		

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SKWBS-200-Cu-PVD Wafer Specifications

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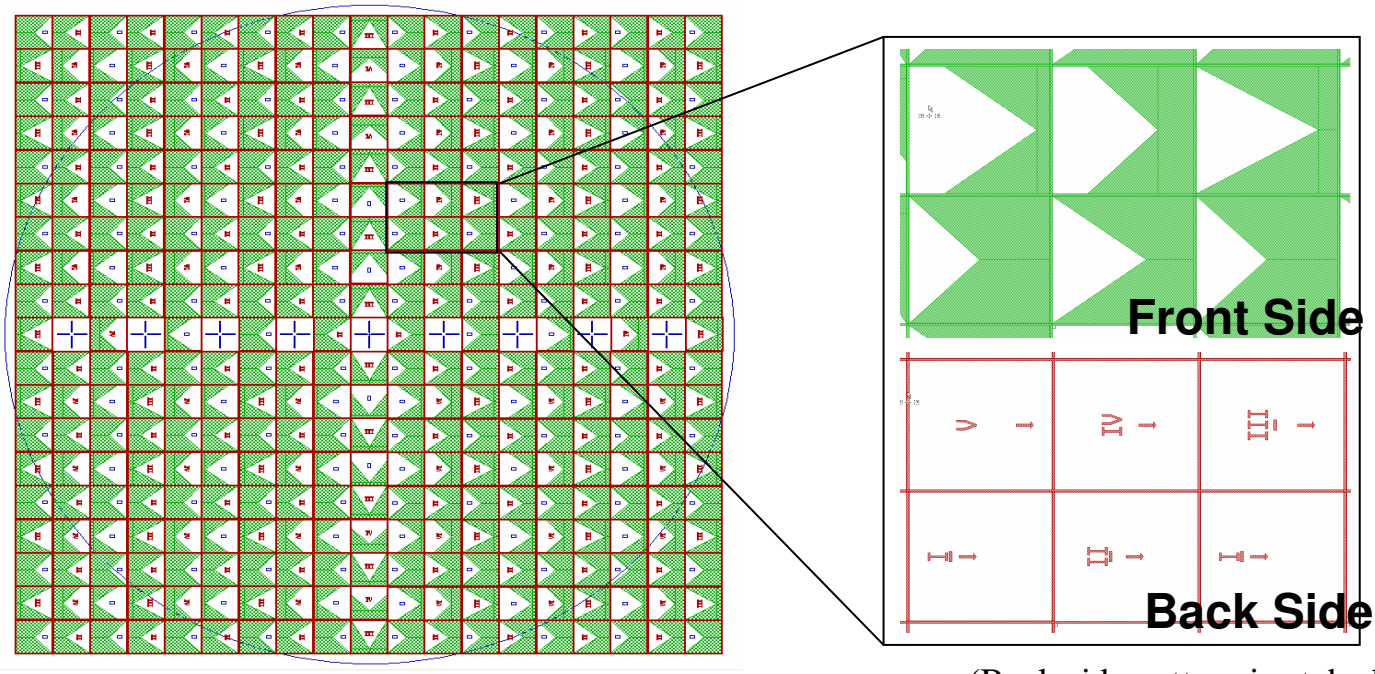
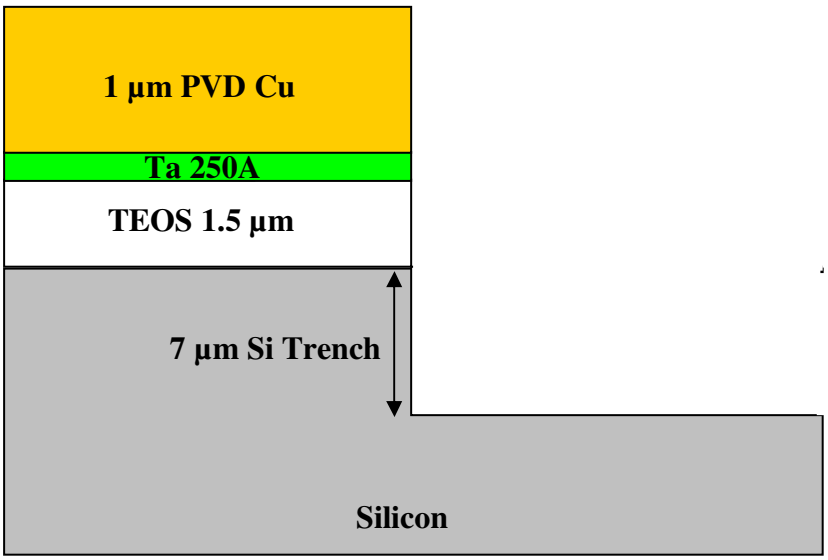


SKWBS-200-Cu-PVD Mask Layout

(Back side pattern is etched 1-2 µm into silicon for dicing reference purposes)



Cross Sectional View

PARAMETER	NOMINAL	TOLERANCE
Patterning		
Die Size: X	10 mm	+/- 10 µm
Die Size: Y	10 mm	+/- 10 µm
Die Stepping (X /Y)	200 / 200 µm	+/- 10%
Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on the wafer unpatterned. (Under certain stepper operating conditions, 2 mm edge edge exclusion is allowed.)		
TEOS Oxide film thickness		
Lot-to-Lot	1.5 µm	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 3 %
Within-Die		+/- 3 %
PVD Ta film thickness		
Lot-to-Lot	250 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
PVD Cu film thickness		
Lot-to-Lot	1 µm	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
Silicon trench depth		
Lot-to-Lot	7 µm	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 10 %
Within-Die		+/- 10 %
Si substrate: p-type (100), resistivity 1-100 ohm-cm, double-side polished		

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SKWBS-200-Ox Wafer Specifications

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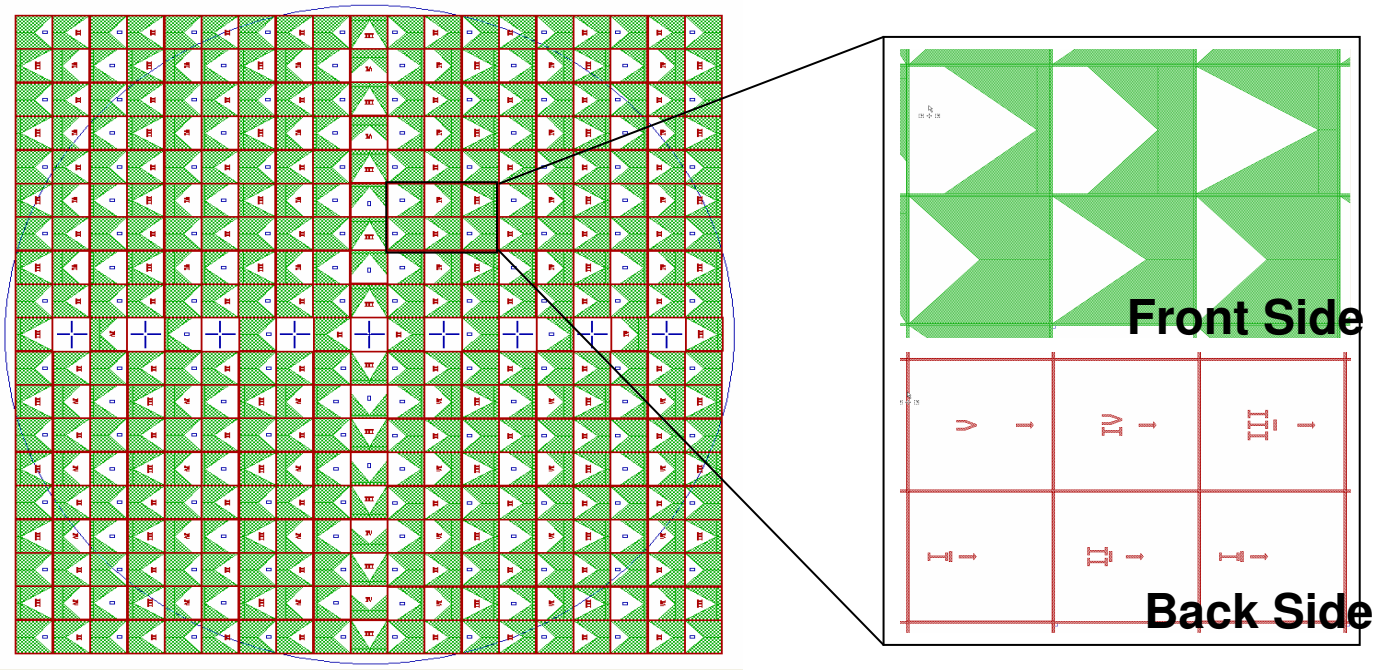
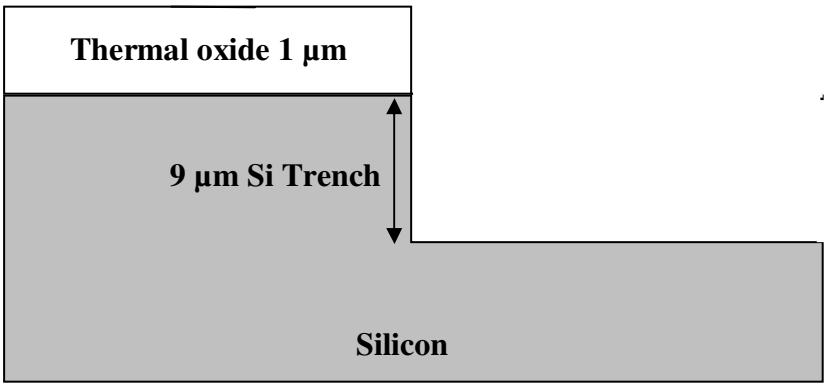


SKWBS-200-Ox Mask Layout

(Back side pattern is etched 1-2 µm into silicon for dicing reference purposes)



Cross Sectional View

PARAMETER	NOMINAL	TOLERANCE
Patterning		
Die Size: X	10 mm	+/- 10 µm
Die Size: Y	10 mm	+/- 10 µm
Die Stepping (X /Y)	200 / 200 µm	+/- 10%
Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on the wafer unpatterned. (Under certain stepper operating conditions, 2 mm edge edge exclusion is allowed.)		
Thermal Oxide film thickness		
Lot-to-Lot	1 µm	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 3 %
Within-Die		+/- 3 %
Silicon trench depth		
Lot-to-Lot	9 µm	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 10 %
Within-Die		+/- 10 %
Si substrate: p-type (100), resistivity 1-100 ohm-cm, double-side polished		

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SKWBS-200-TEOS Wafer Specifications

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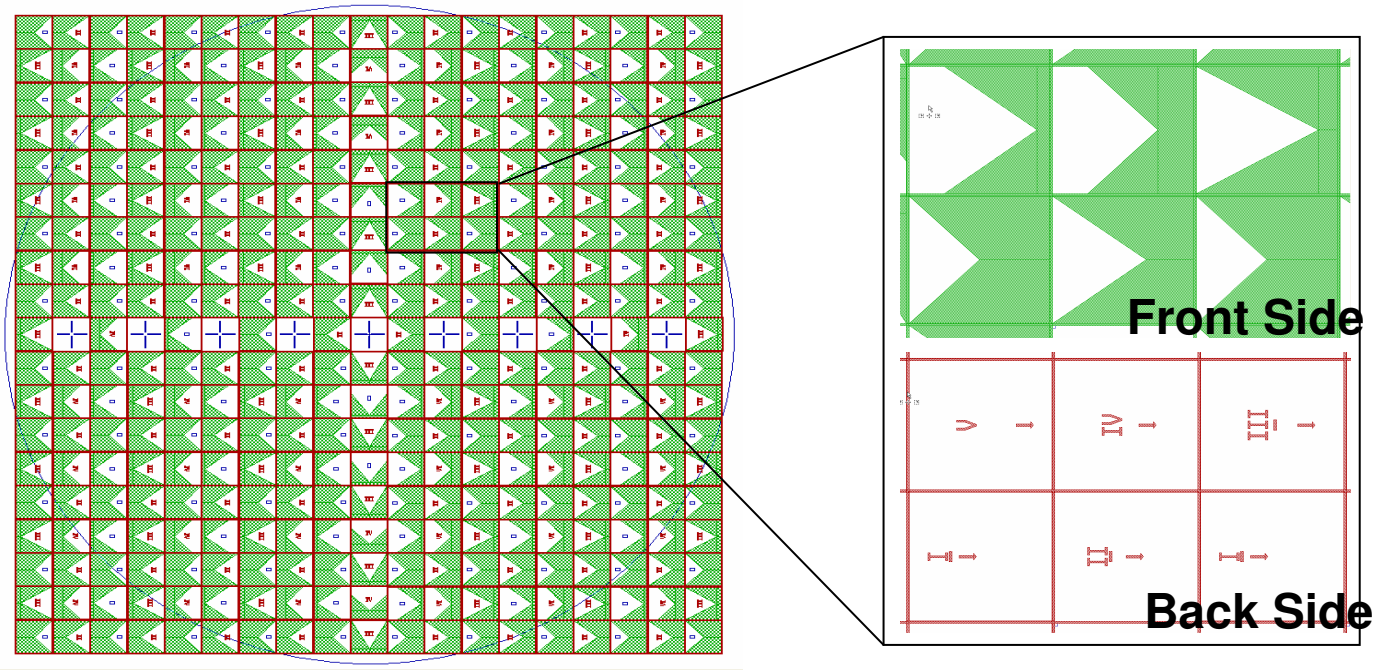
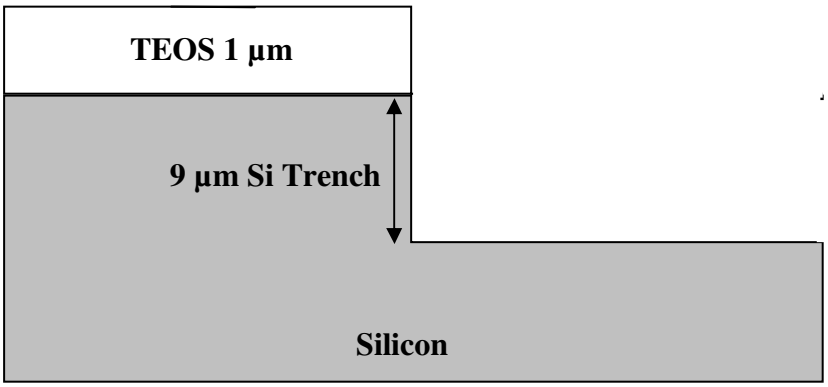


SKWBS-200-TEOS Mask Layout

(Back side pattern is etched 1-2 µm into silicon for dicing reference purposes)



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TEOS Oxide film thickness		
Lot-to-Lot	1 µm	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 3 %
Within-Die		+/- 3 %
Silicon trench depth		
Lot-to-Lot	9 µm	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 10 %
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SKWBS-200-Si Wafer Specifications

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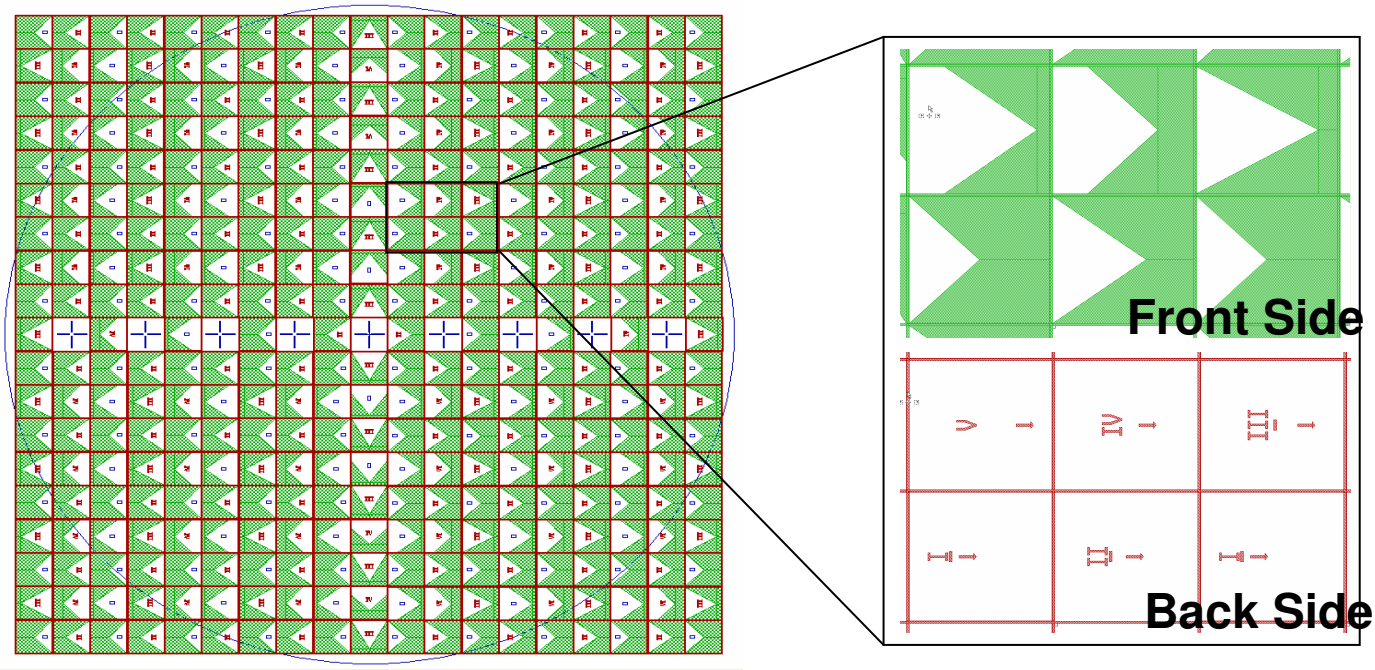

SKWBS-200-Si Mask Layout

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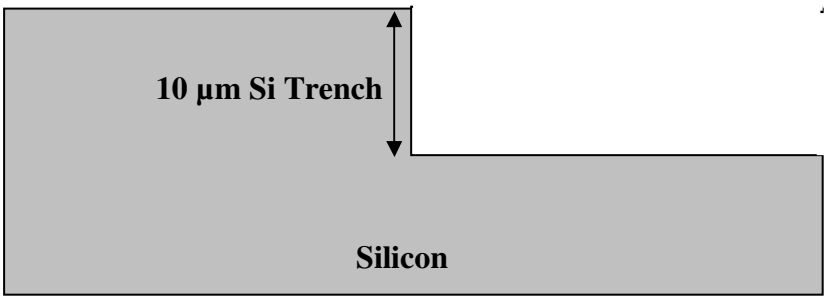

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Patterning		
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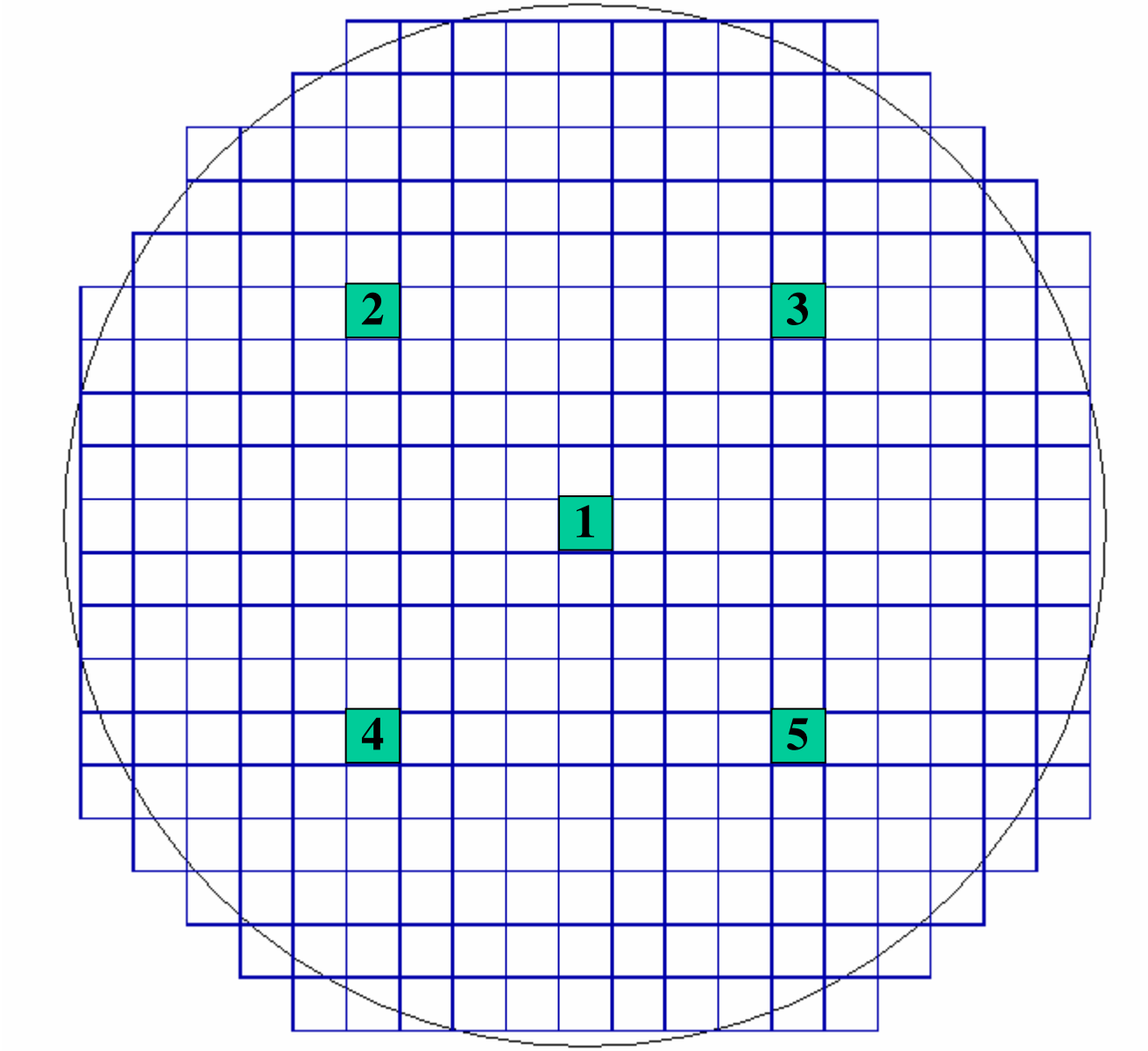
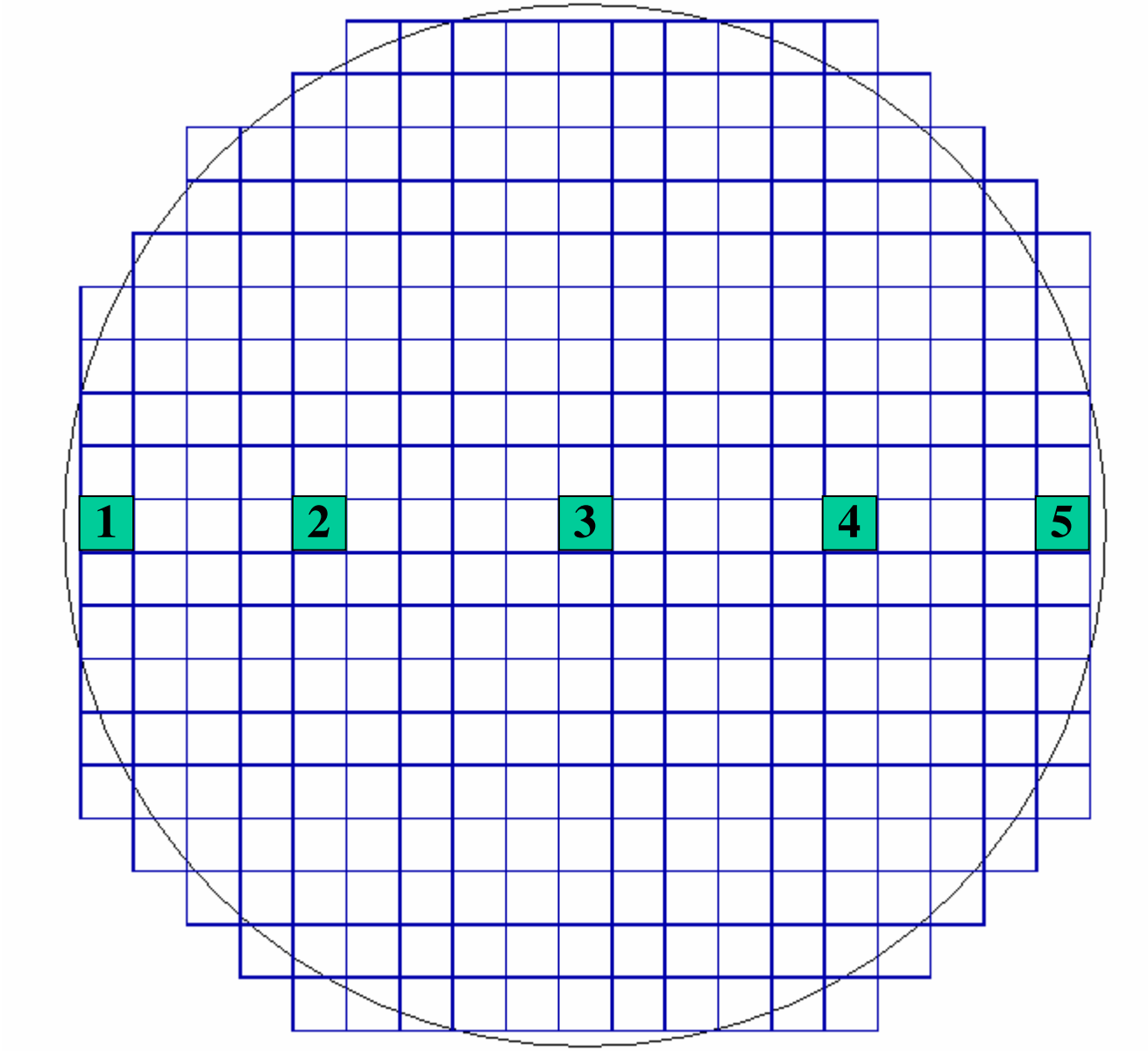
Silicon trench depth		
Lot-to-Lot	10 µm	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 10 %
Within-Die		+/- 10 %
Si substrate: p-type (100), resistivity 1-100 ohm-cm, double-side polished		

SKWBS-200 Bond Strength Measurement Location Map #1



SITE LOCATIONS

SKWBS-200 Bond Strength Measurement Location Map #2



SITE LOCATIONS