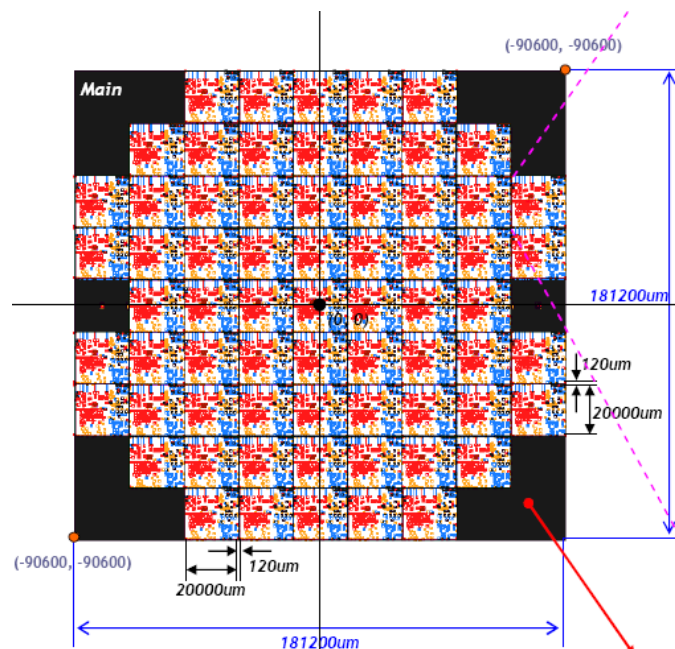
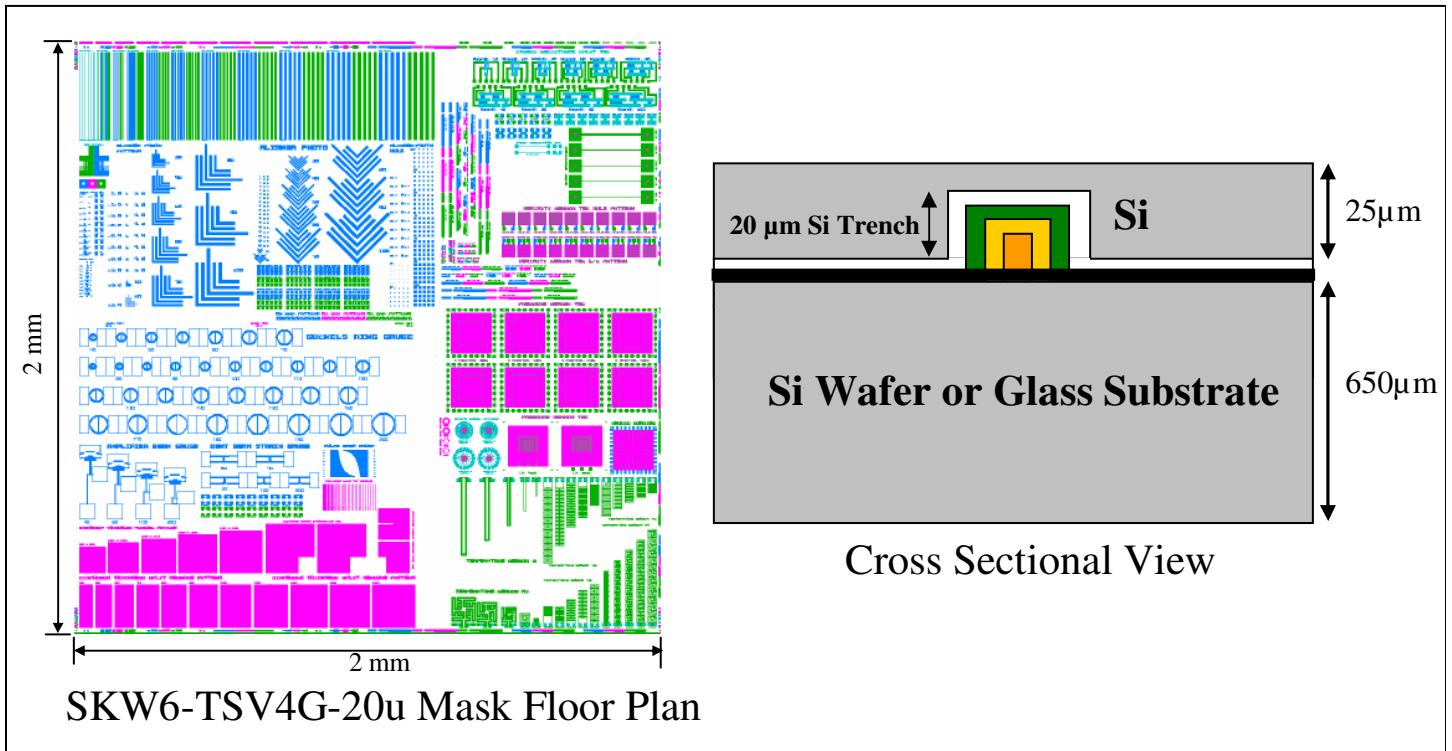


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SKW6-TSV4G-20u Wafer Specifications

DATE: February 8, 2010



SKW6-TSV4G-20u Wafer Die Map

PARAMETER	NOMINAL	TOLERANCE
Patterning		
Die Size: X	2 mm	+/- 10 μm
Die Size: Y	2 mm	+/- 10 μm
Die Stepping (X /Y)	120 / 120 μm	+/- 10%
CD Variation (measured on 10 μm and 50 μm hole structures)		
Lot-to-Lot	10 μm , 50 μm	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
Base silicon substrate thickness		
Lot-to-Lot	650 μm	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 3 %
Within-Die		+/- 3 %
Upper silicon substrate thickness		
Lot-to-Lot	25 μm	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 8 %
Within-Die		+/- 8 %
Silicon Trench Depth		
Lot-to-Lot	20 μm	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 10 %
Within-Die		+/- 10 %
Pad Oxide film thickness		
Lot-to-Lot	3000 Å	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 3 %
Within-Die		+/- 3 %

PARAMETER	NOMINAL	TOLERANCE
PVD TiN film thickness		
Lot-to-Lot	300 Å	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 3 %
Within-Die		+/- 3 %
PVD Cu film thickness		
Lot-to-Lot	1000 Å	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 3 %
Within-Die		+/- 3 %